REMARKS

At the outset, the Examiner is thanked for the review and consideration of the present application. The following remarks are submitted as a full and complete response to the Office Action.

Amendment of Claims

Claim 3 is amended to overcome the objection by the Examiner. In addition, Applicant also amends Claims 1 and 17 and adds new Claims 18-20 in order to clarify the characteristics of the present invention. These amendments are all supported by the original specification as set forth below:

The amended Claim 1:	FIGS. 8-9 as well as paragraphs [0038] and [0039] in the original specification.
The amended Claim 17:	Paragraph [0024] in the original specification.
The new Claim 18:	FIGS. 1-9 in the original specification.
The new Claim 19:	FIG. 8 and paragraph of [0038] in the original specification.
The new Claim 20:	FIG. 9 and Paragraphs [0008], [0039] and [0043] in the original specification.

Therefore, it should be understood that no new matter is introduced by way of the above amendments. The remarks are based on the amended Claims.

Claim Rejections – 35 USC § 103

Claims 1, 3, 4, and 17 are rejected under 35 USC 103(a) as being unpatentable over Ito el al. (US 6,240,632) in view of Kurita et al. (US 6,399,891), with teachings from Saijo et al. (US 6,579,565). Applicant respectfully traverses the rejection for the reason set forth below:

Claim 1 cannot be obtained from the prior art of Ito et al. (US 6,240,632) in view of Kurita et al. (US 6,399,891), and Saijo et al. (US 6,579,565) because this invention is neither taught nor suggested by the combination of references, since the concept of the present invention is totally different from that of Ito et al.

The concept of Ito et al. is directed to a lead frame used to join a semiconductor chip. In this regard, referring to FIGS. 7D-7F and 8G-8H disclosed by Ito et al., the substrate 11 is removed before connecting the electronic component 31 to the Copper lead 17. However, in the present invention, the substrate is removed after connecting the electronic components to the topmost circuit layer as described in Claim 1. The disclosure of Ito et al. is apparently unable to conduct the above step of Claim 1 because the substrate 11 of Ito et al. must be removed first, not only due to the electronic component 31, but also due to the reinforcement plate 33, since both of which are prepared to take the space being occupied by the substrate 11. The electronic component of Claim 1 is placed on the topmost circuit layer rather than taking the space being occupied by the substrate. Therefore, the concept of the present invention is totally different than that of Ito et al.

The addition of Kurito et al. and Saijo et al. does not cure this deficiency of the prior art teaching. Thus, no combination of the cited references teaches or suggests the claimed invention. Accordingly, Applicant requests reconsideration and withdrawal of this rejection to Claims 1, 3, 4, and 17.

Claims 9, 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ito et al. in view of Kurita et al. and Saijo et al., and in further view of Farnworth (U.S. 6,365,501). Applicant disagrees and requests reconsideration and withdrawal of this rejection.

As noted above, Ito et al. teaches away from the claimed invention and no combination of Ito et al., Kurita et al. and Saijo et al. suggests the invention as set forth in Claim 1, from which Claims 9, 11 and 12 depend. The addition of Farnworth does not cure this deficiency. Applicant, therefore, requests reconsideration and withdrawal of this rejection.

Claims 2 and 5-8 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Ito et al. in view of Kurita et al. and Saijo et al., in further view of Ikegami et al. Applicant disagrees.

Since no combination of Ito et al., Kurita et al. and Saijo et al. teaches or suggests the invention set forth in Claim 1 (the combination actually teaches away from the claimed invention), and the addition of Ikegami does not cure this deficiency, no combination of these references teaches or suggests the claimed invention as set forth in Claims 2 and 5-8 that depend from Claim 1. Applicant thus requests withdrawal of this rejection.

Claim 10 stands rejected as being unpatentable over Ito et al. in view of Kurita et al. and Saijo et al. and Ikegami et al., in further view of Farnworth. Applicant disagrees.

As noted above, no combination of these cited references teaches or suggests the invention as set forth in Claim 1, from which Claim 10 depends. Applicant, therefore, requests reconsideration and withdrawal of this rejection to Claim 10.

Claims 13, 15 and 16 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Ito et al. in view of Kurita et al. and Saijo et al., in further view of Lin et al. and Meyrat et al. with teachings from Carey et al. Applicant disagrees.

As noted above, no combination of Ito et al., Kurita et al., Saijo et al. teaches or suggests the elements of Claim 1, from which Claims 13, 15 and 16 depend. The addition of Lin et al.

and Meyrat et al. does not cure this deficiency of the teaching of the references. Applicant therefore requests reconsideration and withdrawal of this rejection to Claims 13, 15 and 16.

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ito et al. in view of Kurita et al., Saijo et al., and Ikegami et al., in further view of Lin et al. and Meyrat et al. In view of the amendments and remarks set forth herein, Applicant requests reconsideration and withdrawal of this rejection.

In addition, Applicant also adds Claims 18-20 for further clarifying additional characteristics different from the disclosure of Ito et al. in combination with the additional cited references. Applicant submits that Ito et al. in any combination with the cited references still fails to disclose or suggest:

(1) the step of "removing the substrate to expose the first circuit layer after the step of applying the encapsulant layer" as recited in Claim 18;

(2) the characteristic of "the electronic component is embedded in the second circuit layer" as recited in Claim 19; and

(3) the step of "applying an encapsulant layer to cover the electronic component and all of the layers above the first circuit layer" as recited in Claim 20.

In the disclosure of Ito et al., as shown in FIG. 8I, the encapsulant layer 36 (only covered the chip 31, a portion of the lead 17, and a portion of PI 21) is unable to support the whole integrated circuit. Thus, the reinforcement plate 33 for supporting the entire integrate circuit is required. However, please note in the present invention (FIGS. 8-10), the encapsulant layer is applied to cover not only the electronic component, but also all the layers above the first circuit layer. This indicates that the encapsulant layer also functions as a support of the integrated circuit. In other words, the substrate can be replaced after forming the encapsulant layer as

recited in Claim 20. As a result, the thickness of the integrated circuit having multiple circuit layers is nearly the thickness of the encapsulant layer (referring to paragraph [0008] of the specification). The disclosure of Ito et al., alone or in combination with the other cited references, nowhere teaches this characteristic.

Conclusion

In view of the above remarks, it should be understood that the independent Claims 1 and 18 are not anticipated or rendered obvious by Ito et al. alone or in combination with the references relied upon by Examiner. Therefore, the rejections of Claims 1 and Claims 2-17 depended thereon are respectfully traversed. All of the claims in the present application are believed to be in condition for allowance. The Applicant respectfully requests that a Notice of Allowance be issued to this application.

Respectfully submitted,

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